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X Utility Patent Application under 37 CFR § 1.53(b) comprising:
- X Specification (25 pgs, including claims numbered 1 through 80 and a 1 page Abstract).
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Local Multilayered Metallization

Field of the Invention

This invention relates to the field of integrated circuit manufacturing, and more particularly to metallization in integrated circuit manufacturing.

Background of the Invention

Copper and copper alloys are often substituted for the more traditional aluminum and aluminum alloys as the primary signal and power carrying conductive structures in integrated circuits. Unfortunately, when copper and copper alloy pads are wire-bonded to a highly conductive wire, such as a gold, using current state-of-the-art wire-bonding processes, the resulting copper and gold bonds or copper alloy and gold bonds are not as reliable as aluminum and gold bonds or aluminum alloy and gold bonds used in the prior art.

One solution to this problem is shown in the prior art bonding structure 100 of Figure 1. Bonding structure 100 includes substrate 103, copper conductor 106, dielectric layer 109, barrier layer 112, aluminum layer 115, passivation layer 116 and polyimide layer 118. To avoid wire-bonding to copper, dielectric layer 109 is etched at the location of copper conductor 106, and a barrier layer 112 of titanium or titanium nitride is deposited above copper conductor 106. Aluminum layer 115 is deposited above barrier layer 112, and passivation 116 and polyimide layers 118 are deposited above aluminum layer 115. Finally, passivation 116 and polyimide 118 layers are etched to expose aluminum layer 115 for wire-bonding. Unfortunately, this solution has several problems. First, it requires two extra masking operations that are not required when wire-bonding to an aluminum or an aluminum-copper conductor. It requires a masking operation to expose copper conductor 106 prior to depositing barrier layer 112 and aluminum layer 115, and it requires a masking operation to pattern aluminum layer 115, prior to wire-bonding. Second, the extra processing steps increase the complexity of the manufacturing operation and the failure rate of the manufactured circuits. Third, the

solution is expensive, since it requires more materials, masking steps, and time than the prior art processes to manufacture the integrated circuit.

For these and other reasons there is a need for the present invention.

Summary of the Invention

The above mentioned problems with integrated circuit metallization and other problems are addressed by the present invention and will be understood by reading and studying the following specification.

An interconnect comprising a trench and a number of metal layers above the trench is disclosed. The trench has a depth and a width. The depth is greater than a critical depth, and the number of metal layers is determined by the width.

In an alternate embodiment, a metallization structure having a trench including a metal layer and a second trench including a plurality of metal layers coupled to the metal layer is disclosed. The metal layer is highly conductive, and at least one of the plurality of metal layers is a metal layer that is capable of being reliably wire-bonded to a gold wire. The trench is narrower than the second trench, and at least one of the plurality of metal layers is copper or a copper alloy.

Brief Description of the Drawings

Figure 1 is a cross-sectional side view of a prior art metallization bonding structure.

Figure 2 is a cross-sectional side view of a substrate having trenches and barrier and copper metallization deposited on the substrate.

Figure 3 is a cross-sectional side view of a substrate having a barrier layer and a conductive layer deposited above a copper layer on the substrate.

Figure 4 is cross-sectional side view of a substrate having a filled bond pad trench and a filled signal carrying trench after chemical mechanical polishing.

Figure 5 is a cross-sectional side view of a substrate after opening holes in the passivation and wire bonding.

Figure 6 is a top view of fine lines and wide lines coupled together.

Figure 7 a block diagram of a computer system suitable for use in connection with the present invention.

Detailed Description of the Preferred Embodiments

In the following detailed description of the preferred embodiments, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific preferred embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that logical, mechanical and electrical changes may be made without departing from the spirit and scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims.

Figure 2 is a cross-sectional side view of one embodiment of the invention. In the substrate 200 there will be various implants such as NWELLs, PWELLs, transistor implants, and source-drain implants that are, for simplicity, not shown. Over the substrate 200 may be formed transistor gates, polysilicon or tungsten plugs, and contact holes from the first layer of metallization down to these underlying layers and the silicon substrate. For simplicity, none of these details are shown as they are elements that are well known and may also be present. Over these structures and over the substrate 200 is shown an insulating layer 202. A conductive layer 250 is shown formed in insulating layer 202. Insulating layer 209 is deposited above conductive layer 250 and above the insulating layer 202. If the top surface defined by insulating layer 202 and conductive layer 250 is not globally planar, then the top surface of insulating layer 209 will need to be made globally planar by chemical mechanical polishing (CMP). Openings 210 (in the insulating layer 209) to the conductive layer 250 are formed by patterning and etching.

Next, trenches 215, 218, 221 are etched into the insulating layer. Barrier layer 224, seed layer 227, and copper layer 230 are then deposited into these trenches.

What is shown in Figure 2 is a double damascene process in which both the opening 210 and the trenches 215, 218, 221 are patterning into the insulating layer 209

prior to depositing any metal layers. As is well known in the art, a single damascene process could have been shown. Trench 221 is the bonding pad trench.

Substrate 200 is a semiconductor, such as silicon or germanium, or other material, such as gallium arsenide or silicon-on-sapphire, suitable for use as a substrate in the fabrication of integrated circuits.

Insulating layer 209 is deposited above substrate 200. Insulating layer 209 blocks undesired current flow between the substrate 200 and the conductive layers above insulating layer 209. Insulating layer 209 additionally serves to block current flow between distinct conductive lines patterned into the insulating layer 209. Insulating layer 209 is not limited to a particular insulating material. In one embodiment, insulating layer 209 is an oxide, such as silicon oxide, fluorinated silicon oxide, or silicon dioxide. In an alternate embodiment, insulating layer 125 is a polymer, a foamed polymer, or polyimide. After insulating layer 209 is deposited on conductive layer 250 and insulating layer 202, the surface of insulating layer 209 may be planarized using a surface planarizing process, such as chemical mechanical polishing. This planarization of layer 209 is required if the top surface of the underlying insulating layer 202 and conductive layer 250 was not previously planarized. The insulating layer has a final thickness 233.

Trenches or depressions 215, 218, 221 are etched in insulating layer 209 and when filled with a conductive material are capable of functioning as electrical interconnects, signal carrying conductors, conductive structures, or connective structures coupling together integrated circuit elements, such as resistors, capacitors, and transistors, or coupling integrated circuit elements to bonding pads. These electrical interconnects are also suitable for use in connection with the fabrication of memory circuits or cells, logic circuits or cells, and analog circuits or cells. Trenches 215 and 218 are etched to dimensions suitable for a signal carrying conductor. All trenches 215, 218, 221 are etched to a depth 236. Signal carrying conductor filled trench 215 has a width 239 and a depth 236. Width 239 and depth 236 are selected to provide a particular resistance and capacitance for the conductor. Since the resistance of a conductor is inversely proportional to the cross-sectional area of conductor, the greater the depth 236 and width 239 of trench 215, the less the resistance of the conductor that fills the trenches.

The widths of trenches 215 and 218 are not limited to a particular value. For example, in one embodiment, trench 215 is etched to a width 239 that is less than the width 244 of bonding pad trench 221. Restricting the width of trenches 215 and 218 to a width that is less than the width of bonding pad trench 221 permits trenches 215 and 218 to overfill during a copper deposition process, while bonding pad trench 221 under fills.

Trench 221 is a bond pad. Trench 221, in one embodiment, is etched to dimensions sufficient for use in a wire-bonding operation, and trench 221 is etched to a width 244 that is greater than the width 239 of trench 215 and the width of trench 218.

Critical width 290, in one embodiment, is defined as twice the sum of the side wall barrier thickness 280, the sidewall seed thickness 284, and the sidewall copper thickness 288 (i.e., critical width 290, equals 2x[sidewall barrier thickness 280 + sidewall seed thickness 284 + sidewall copper thickness 288]).

The minimum trench width 239 is less than or equal to the critical width 290. The bond pad trench 244 is greater than the critical width 290.

The process flow shown in Figures 2, 3, and 4 is a dual damascene process. In this process the opening 210 and the trenches 215, 218, 221 are formed in the insulating layer 209. Then the metallization layers are deposited to simultaneously deposit into the opening 210 and the trenches 215, 218, 221. A variety of devices, such as memory cells, logic cells, capacitors, and transistors, can be interconnected using a dual damascene process with a copper interconnect.

Alternatively, a simple damascene process may be used. In the simple damascene process, openings are formed in an insulating layer down to a conducting layer. The opening is then filled with a conducting material such as Ti/TiN/W. This Ti/TiN/W deposition is removed from the surface of the insulating layer by dry etch, wet etch, or CMP to leave the Ti/TiN/W metal sandwich structure in the openings only. Next, another insulating layer is deposited and trenches are etched through this insulating layer, so that a trench exposes the top surface of the Ti/TiN/W metallization in an opening. The trenches are then deposited with a second metallization. After a subsequent metal dry etch or CMP, the damascene metallization in the trenches is formed.

Barrier layer 224 is deposited above insulating layer 209 to block the diffusion of copper into insulating layer 209. In one embodiment, barrier layer 224 is fabricated from titanium and titanium nitride. In an alternate embodiment, barrier layer 224 is fabricated from tantalum. In another alternate embodiment, barrier layer 224 is fabricated from tantalum nitride. In still another alternate embodiment, barrier layer 224 is fabricated from tantalum and tantalum nitride. Barrier layer 224 is deposited to a thickness of between about 50 and about 1000 angstroms. Forming a barrier layer 224 having a thickness of less than about 50 angstroms does not adequately block the flow of impurities into insulating layer 209. Forming barrier layer 224 with a thickness of more than about 1000 angstroms tends to leave insufficient space in trenches 215 and 218 for a conductive material. In the preferred embodiment, barrier layer 224 is formed from tantalum nitride deposited to a thickness of between about 100 and 500 angstroms. In the preferred embodiment, barrier layer 224 is deposited by chemical vapor deposition (CVD). Alternatively, barrier layer 224 is deposited by a physical vapor deposition technique, such as sputtering.

Seed layer 227, in one embodiment, is formed from a conductive material deposited on barrier layer 224 to provide a site for depositing a metal to form an integrated circuit interconnect. In an alternate embodiment, seed layer 227 is formed from copper. In another an alternate embodiment, seed layer 227 is formed from an alloy of copper, such as CuAl. Seed layer 227 is deposited by physical vapor deposition or chemical vapor deposition to a depth that is sufficient to support an electroplating deposition process. In one embodiment, a seed layer of copper is deposited to a depth of between about 100 and 1000 angstroms. In still another alternate embodiment of an interconnect, seed layer 227 is not formed, and copper layer 230 is formed above barrier layer 224.

Copper layer 230, in one embodiment, is formed above the barrier layer 224 and the seed layer 227. In one embodiment, copper layer 230 is fabricated from copper or an alloy of copper, such as CuAl. Copper layer 230 is deposited above the barrier layer 224 and the seed layer 227 to a depth that overfills trenches 215 and 218, while under filling bond pad trench 221. In the preferred embodiment, copper layer 230 is deposited by

electroplating. In an alternate embodiment, copper or copper alloy is deposited by CVD or sputtering. The depth of the copper deposited in trenches 215, 218, 221 is controlled by adjusting the deposition process. In one embodiment, trenches 215 and 218 are filled or overfilled, while trench 221 is under filled to permit latter filling with a material suitable for eutectically bonding to a gold wire using state-of-the-art wire-bonding processes.

Figure 3 is a cross-sectional side view of substrate 200 having a barrier layer 300 deposited above copper layer 230 and a conductive layer 303 deposited above barrier layer 300. Barrier layer 300 is fabricated from a material that blocks the migration of copper into conductive layer 303. In one embodiment, barrier layer 300 is fabricated from a material, such as a refractory metal, TiN, TaN, Ti/TiN, Ta/TaN, or Ti/TaN. Conductive layer 303 is fabricated from a material that is easily and reliably wire-bonded using state of the art wire-bonding processes. In one embodiment, conductive layer 303 is fabricated from aluminum. In an alternate embodiment, conductive layer 303 is fabricated from an alloy of aluminum, such as AlCu. Conductive layer 303 is deposited on barrier layer 300 to a depth that is sufficient to wire-bond to a gold wire.

As shown in Figure 3, the vertical barrier thickness 382 is the thickness of the barrier layer 224 at the bottom of a wide trench such as the bond pad trench 221. The vertical seed thickness 384 is the thickness of the seed layer 227 at the bottom of a wide trench such as the bond pad trench 221. The vertical copper thickness 386 is the thickness of the copper layer 230 at the bottom of a wide trench such as the bond pad trench 221. The vertical barrier thickness 388 is the thickness of the barrier layer 300 at the bottom of a wide trench such as the bond pad trench 221.

Critical depth 390, in one embodiment, is defined as follows: Critical depth 390 = the vertical barrier thickness 382 + vertical seed thickness 384 + vertical copper thickness 386 + vertical barrier thickness 388.

The trench depth 236 must be greater than the critical depth 390.

Figure 4 is cross-sectional side view of substrate 200 of Figure 3 after chemical mechanical polishing (CMP). CMP removes unwanted layers of metal from the surface of insulating layer 209. After CMP, the copper filling trenches 215 and 218 is flush with

the surface of insulating layer 209. Also, after CMP, bonding pad trench 221 is partially filled by copper layer 230 and partially filled with conductive layer 303. Copper layer 230 and conductive layer 303 are flush with the surface of insulating layer 209 if the deposited thickness of conductive layer 303 is sufficient to finish filling the trench 221.

After chemical mechanical polishing of the metal stack layers 224, 227, 230, 300, 303, in one embodiment, a passivation layer 309 is deposited. This passivation layer may be oxide, nitride, oxide/nitride, nitride/oxide/nitride, polyimide, or any combination. The passivation layer is patterned and etched to create openings in the bond pad trench 221 exposing the conductive layer 303 as shown in Figure 5. Wire bonds are then attached to conductive layer 303 through the openings in the passivation as shown in Figure 5. In one embodiment, conductive layer 303 is a material that easily and reliably bonds with gold, such as aluminum or an aluminum copper alloy containing about one-half percent copper. Gold conductor 403 is wire-bonded to bonding material 400 to couple the bonding pad formed in trench 221 to an external connector.

In summary, given a metallization stack of n layers, each with bottom thickness t_{b1}, t_{b2}, t_{b3}, ..., t_{bn} and each with sidewall thickness t_{s1}, t_{s2}, t_{s3},..., t_{sn}, so long as the trench depth is greater than the

$$\textbf{critical depth} = \sum_{i=1}^{n-1} t_{bi}$$

then the number of layers in the metal stack in each trench will depend on the trench width. For example, for a metallization stack comprised of only metal layers and for trenches having a width $< 2t_{s1}$, the trench will be completely filled with a first metal. For trenches having $2t_{s1} <$ width $< 2(t_{s1} + 2t_{s2})$, the trench will contain a first metal layer and a second metal layer, but not any subsequently deposited metal layers. In this way, a plurality of trenches are easily formed with different metallizations programmed by defining the trench width.

An advantage of local multilayered metallization in bond pad trench 221 is that reliable wire-bonding using current state-of-the-art wire-bonding processes is enabled without adding masking steps to the integrated circuit manufacturing process.

Figure 6 is a top view of fine line 603 coupled to wide lines 606 and 609. In one embodiment, fine line 603 is a signal carrying line and wide lines 606 and 609 are bonding pads for coupling signal carrying line 603 to off chip connectors 612 and 615. Off chip connector 612 is coupled to wide line 606 by conductive wire 618, and off chip connecter 615 is coupled to wide line 609 by conductive wire 621. Conductive wires 618 and 621 are fabricated from a conductor such as gold, and are coupled to wide lines 606 and 609 using wire-bonding techniques. In one embodiment, wide lines 606 and 609 have a surface layer of aluminum or an aluminum-copper alloy. The bond formed between the aluminum gold wire or between the aluminum-copper alloy and the gold wire is more reliable and stronger than a wire bond between gold and copper. The process for the fabrication of fine line 603 and wide lines 606 and 609 is described above.

Figure 7 a block diagram of a computer system 700 suitable for use in connection with the present invention. System 700 comprises processor 705 and memory device 710, which includes conductive structures and interconnects of one or more of the types described above in conjunction with Figures 1-6. The conductive structures and interconnects of the present invention are capable of coupling logic cells, logic devices, and integrated circuits commonly found in processor 705, such as a microprocessor, a reduced instruction set processor, or a parallel processor. The conductive structures and interconnects of the present invention are also capable of coupling memory devices, memory cells, and integrated circuit memories commonly found in memory device 710. Memory device 710 comprises memory array 715, address circuitry 720, and read circuitry 730, and is coupled to processor 705 by address bus 735, data bus 740, and control bus 745. Processor 705, through address bus 735, data bus 740, and control bus 745 communicates with memory device 710. In a read operation initiated by processor 705, address information, data information, and control information are provided to memory device 710 through busses 735, 740, and 745. This information is decoded by addressing circuitry 720, including a row decoder and a column decoder, and read circuitry 730. Successful completion of the read operation results in information from memory array 715 being communicated to processor 705 over data bus 740.

Conclusion

Several embodiments of a conductive structure and methods suitable for use with copper interconnects and state-of-the-art wire bonding systems have been described. These embodiments permit highly reliable wire-bonding connections between chip bond pads and package interconnects. Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. Therefore, it is intended that this invention be limited only by the claims and the equivalents thereof.

What is claimed is:

1. An interconnect comprising:

a trench having a depth and a width, the depth being greater than a critical depth; and

a number of metal layers above the trench, wherein the number of metal layers is determined by the width.

2. The interconnect of claim 1, further comprising:

a number of metal stack layers including the number of metal layers above the trench, wherein the number of metal stack layers has a thickness, and the critical depth is equal to a second thickness of a second number of metal stack layers equal to one less than the number of metal stack layers.

3. The interconnect of claim 2, wherein at least one of the number of metal layers is fabricated from copper.

4. An interconnect comprising:

a trench having a width and a depth, the depth being greater than a critical depth;

a number of metal stack layers capable of defining a critical width and located above the trench; and

a number of metal layers above the trench, wherein the number of metal layers above the trench is a function of the width and the critical width.

5. The interconnect of claim 4, wherein the width is greater than the critical width.

6. The interconnect of claim 4, wherein each of the number of metal stack layers is planarized by chemical mechanical polishing.

7. An interconnect comprising:

a trench having a depth and a width; and

a number of metal layers above the trench, wherein for the depth being greater than a critical depth, the number of metal layers are capable of being increased as the width increases.

8. An interconnect comprising:

a trench having a trench depth greater than a critical depth;

a number of metal stack layers above the trench, the number of metal stack layers having a thickness; and

a number of metal layers above the trench, wherein the number of metal layers is capable of being increased as the thickness decreases.

9. The interconnect of claim 8, wherein at least one of the number of metal stack layers above the trench couples a first logic device to a second logic device.

10. An interconnect comprising:

a first memory cell;

a second memory cell;

a trench having a trench depth greater than a critical depth; and

a number of metal stack layers above the trench, wherein each of the number of metal stack layers has a sidewall thickness, the number of metal stack layers above the trench is capable of being increased as the sidewall thickness decreases, and at least one of the number of metal stack layers couples the first memory cell to the second memory cell.

11. An interconnect comprising:

a first trench having a depth greater than a critical depth and a width less than twice a first sidewall thickness;

a second trench having the depth of the first trench and a width greater than twice the first sidewall thickness and less than twice a sum of the first sidewall thickness and a second sidewall thickness;

a first metal layer above the first trench and the second trench; and

a second metal layer above the second trench.

12. The interconnect of claim 11, wherein the first metal layer above the first trench couples a first integrated circuit device to a second integrated circuit device in a memory module.

13. The interconnect of claim 11, wherein the first metal layer above the first trench couples a first integrated circuit device to a second integrated circuit device in a logic module.

14. The interconnect of claim 11, wherein the second metal layer is fabricated from Al-Cu.

15. An interconnect comprising:

a first trench having a top and a depth greater than a critical depth, and a width less than a sidewall width of a first metal;

a second trench having a depth greater than a second critical depth, and a width greater than twice the sidewall width of the first metal and less than twice a sidewall width of a second metal; and

a first and a second metal deposited on the first trench and the second trench, the second metal is planarized to the top of the first trench.

16. The interconnect of claim 15, wherein the second metal comprises Al.

17. The interconnect of claim 15, wherein the second metal is planarized by chemical mechanical polishing.

18. A method for forming an interconnect comprising:

selecting an insulative surface;

selecting a number of metallization stack layers having a critical thickness;

etching a trench on the insulative surface, the trench having a depth greater than the critical thickness and a width less than a sidewall thickness of a first metallization stack, and the trench coupling a first memory cell to a second memory cell;

etching a second trench on the insulative surface, the second trench having a depth greater than the critical thickness and a width greater than the sidewall thickness and less than a second sidewall thickness of a second metallization stack;

depositing the first metal layer;

depositing the second metal layer; and

planarizing the insulative surface.

19. The method of claim 18, wherein depositing a first metal comprises depositing copper.

20. The method of claim 18, wherein planarizing the insulative surface comprises planarizing by chemical mechanical polishing.

21. A method for dimensioning a trench comprising:

selecting a number of layers, the number of layers having a sidewall thickness;

selecting a second number of layers having a second sidewall thickness, wherein the second number of layers has one less metal layer than the number of layers;

identifying a critical depth; and

dimensioning the trench to have a depth greater than the critical depth and a width less than the sidewall thickness but greater than the second sidewall thickness.

22. The method of claim 21, wherein identifying a critical depth comprises:

calculating a total bottom thickness for one less layer than the number of layers, the total bottom thickness being the critical depth.

23. An interconnect comprising:

a trench having a width and a metal layer; and

a second trench having a depth greater than a critical depth and a second width greater than the width, the second trench having a plurality of metal layers and at least one of the plurality of metal layers is coupled to the metal layer.

24. The interconnect of claim 23, further comprising a wire bond coupling a conductive material to at least one of the plurality of metal layers.

25. The interconnect of claim 24, wherein at least one of the plurality of metal layers is aluminum.

26. An interconnect comprising:

a trench having a depth greater than a critical depth and a copper layer; and

a second trench wider than the trench, and the second trench having a plurality of metal layers, wherein at least one of the plurality of layers is an aluminum layer, and at least one of the plurality of metal layers is coupled to the copper layer.

27. The interconnect of claim 26, wherein the aluminum layer is an aluminum alloy layer.

28. The interconnect of claim 26, wherein at least one of the plurality of metal layers is a copper layer.

29. The interconnect of claim 26, wherein the aluminum layer is wire-bonded to a conductive material.

30. The interconnect of claim 29, wherein the conductive material is gold.

31. An interconnect comprising:

a trench having a critical depth, a width, a barrier layer, and a metal layer over the barrier layer; and

a second trench having a second width greater than the width and the second trench having a barrier layer, a copper layer over the barrier layer, a titanium layer over the copper layer, a titanium nitride layer over the titanium layer, and an aluminum alloy layer over the titanium nitride layer.

32. The interconnect of claim 31, wherein the barrier layer comprises TiN.

33. The interconnect of claim 31, wherein the aluminum alloy layer is planarized by chemical mechanical polishing.

34. An interconnect comprising:

a trench, a barrier layer, and a metal layer over the barrier layer; and

a second trench, a barrier layer, a copper layer over the barrier layer, a tantalum layer over the copper layer, a tantalum nitride layer over the tantalum layer, and an aluminum alloy layer over the tantalum nitride layer.

35. The interconnect of claim 34, wherein the barrier layer comprises Ti/TiN.

36. A conductive structure comprising:

a trench having a barrier layer and a metal layer over the barrier layer; and

a second trench wider than the trench and the second trench having a barrier layer, a copper layer over the barrier layer, a tantalum layer over the copper layer, a tantalum nitride layer over the tantalum layer, and an aluminum alloy layer over the tantalum nitride layer.

37. The conductive structure of claim 36, wherein the barrier layer comprises TaN.

38. The conductive structure of claim 36, wherein the aluminum alloy layer comprises Al-Si-Cu.

39. The conductive structure of claim 36, wherein the copper layer is planarized by chemical mechanical polishing.

40. A conductive structure comprising:

a trench having a barrier layer and a metal layer over the barrier layer; and

a second trench having a depth greater than a critical depth, a barrier layer, a copper layer over the barrier layer, a tantalum layer over the copper layer, and an aluminum alloy layer over the tantalum layer.

41. The conductive structure of claim 40, wherein the metal layer is copper.

42. The conductive structure of claim 40, wherein the aluminum alloy is aluminum-copper.

43. The conductive structure of claim 40, wherein the barrier layer is Ta/TaN.

44. An interconnect comprising:

a trench having a width and a barrier layer and a metal layer over the barrier layer; and

a second trench having a barrier layer, a copper layer over the barrier layer, a tantalum nitride layer over the copper layer, and an aluminum alloy layer over the tantalum nitride layer.

45. The interconnect of claim 44, wherein the second trench has a second width greater than the width.

46. The interconnect of claim 45, wherein the barrier layer is a refractory metal nitride.

47. The interconnect of claim 46, wherein the tantalum nitride layer is planarized by chemical mechanical polishing.

48. An interconnect comprising:

a trench having a depth less than a critical depth and a width less than a critical width and a metal layer; and

a second trench having a depth greater than a critical depth;

a plurality of metal layers above the second trench, at least one of the plurality of metal layers is coupled to the metal layer, wherein at least one of the plurality of metal layers is capable of forming a highly reliable eutectic bond to a conductive material.

49. The interconnect of claim 48, wherein the metal layer is copper.

50. The interconnect of claim 49, wherein at least of the plurality of metal layers is aluminum.

51. The interconnect of claim 48, wherein at least one of the plurality of metal layers is an aluminum alloy.

52. An interconnect comprising:

a trench having a metal layer and a depth greater than a critical depth; and

a second trench having a plurality of metal layers, at least one of the plurality of metal layers is coupled to the metal layer, wherein only one of the plurality of metal layers is capable of forming a highly reliable eutectic bond to a gold wire.

53. The interconnect of claim 52, wherein the second trench has a depth greater than the critical depth.

54. A conductive structure comprising:

a trench having a width, a depth, and a metal layer; and

a second trench having a width, a depth and a plurality of metal layers, the width of the second trench is greater than the width of the trench, and at least one of the plurality of the metal layers is capable of being electrically coupled to the metal layer.

55. The conductive structure of claim 54, wherein at least one of the plurality of the metal layers is wire-bonded to a highly conductive wire.

56. The conductive structure of claim 55, wherein the highly conductive wire is a gold alloy.

57. A conductive structure comprising:

a narrow trench having a metal layer and a depth greater than a critical depth; and

a wide trench having a plurality of metal layers and a second depth equal to the depth, wherein at least one of the plurality of metal layers is coupled to the metal layer.

58. An interconnect comprising:

a trench having a width less than a critical width, a depth and a metal layer; and

a wide depression having a second width greater than the critical width, a second depth equal to the depth, and a plurality of metal layers, wherein at least one of the plurality of metal layers is coupled to the metal layer.

59. The interconnect of claim 58, wherein the depth is greater than a critical depth.

60. The interconnect of claim 59, wherein at least one of the plurality of metal layers is eutectically wire-bonded to a gold wire.

61. A method of forming a conductive structure comprising:

etching a trench having a depth greater than a critical depth in a substrate having a surface;

under filling the trench with a first conductive material;

overfilling the trench with a second conductive material suitable for high reliability wire-bonding; and

polishing the substrate until the first conductive material and the second conductive material are removed from the surface of the substrate.

62. The method of claim 61, wherein polishing the substrate until the first conductive material and the second conductive material are removed from the surface of the substrate comprises:

applying chemical mechanical polishing to remove the first conductive material and the second conductive material from the surface of the substrate.

63. A method of forming a conductive structure comprising:

etching a fine line trench to a depth greater than a critical depth in a substrate having a surface;

etching a wide line trench to the depth in the substrate such that the wide line trench intersects the fine line trench;

filling the fine line trench with a first conductive material;

under filling the wide line trench with the first conductive material;

filling the wide line trench with a second conductive material suitable for high reliability wire-bonding; and

polishing the substrate until the first conductive material and the second conductive material are removed from the surface of the substrate.

64. The method of claim 63, wherein filling the fine line trench with a first conductive material comprises:

overfilling the fine line trench with a first conductive material.

65. The method of claim 63, wherein filling the wide line trench with a second conductive material suitable for high reliability wire-bonding comprises:

under filling the wide line trench with a second conductive material suitable for high reliability wire-bonding

66. A method of forming a conductive structure comprising:

etching a wide line trench having a depth greater than a critical depth in the substrate;

depositing a seed layer above the surface of the substrate;

depositing a layer of conductive material above the seed layer such that the conductive material under fills the wide line trench;

depositing a barrier layer above the layer of conductive material;

depositing a second layer of conductive material above the barrier layer, the second layer of conductive material is capable of reliably wire bonding to a gold wire; and

removing the seed layer, the layer of conductive material, the barrier layer, and the second layer of conductive material from the surface of the substrate.

67. The method of claim 66, wherein depositing a layer of conductive material above the seed layer such that the conductive material under fills the wide line trench comprises:

electroplating a layer of copper above the seed layer such that the copper under fills the wide line trench.

68. The method of claim 66, wherein depositing a second layer of conductive material above the barrier layer, the second layer of conductive material is capable of reliably wire bonding to a gold wire comprises:

depositing a layer of aluminum above the barrier layer, the aluminum layer is capable of reliably wire bonding to a gold wire.

69. A computer system comprising:

a processor;

a device coupled to the processor; and

a interconnect coupled to the device, the interconnect comprising:

a trench having a depth greater than a critical depth and a metal layer; and

a bond pad trench having a bond pad depth equal to the depth and a plurality of metal layers coupled to the metal layer.

70. The computer system of claim 69, further comprising:

a conductive wire eutectically bonded to at least one of the plurality of metal layers.

71. A computer system comprising:

a processor;

a device coupled to the processor; and

a connective structure coupled to the device, the connective structure comprising:

a trench having a depth greater than a critical depth, a barrier layer, and a copper layer above the barrier layer;

a bond pad trench having a barrier layer, the bond pad trench having a copper layer above the barrier layer, and the bond pad trench having a titanium layer above the copper layer, and an aluminum-copper layer above the titanium layer.

72. A computer system comprising:

a processor;

a device coupled to the processor; and

an interconnect coupled to the device, the interconnect comprising:

a fine line having a conductive layer; and

a wide line having a number of conductive layers, and at least one of the number of conductive layers of the wide line being coupled to the fine line.

73. The computer system of claim 72, wherein the wide line is capable of being reliably wire bonded to a conductive gold wire.

74. A computer system comprising:

a processor;

a device coupled to the processor; and

an interconnect coupled to the device, the interconnect comprising:

a fine line having a depth greater than a critical depth, a barrier layer and a layer of electroplated copper; and

a wide line having a wide line depth equal to the depth, a number of conductive layers, and at least one of the number of conductive layers coupled to the electroplated copper.

75. The computer system of claim 74, wherein at least one of the number of conductive layers is wire-bonded to a gold wire.

76. The computer system of claim 74, wherein a eutectic bond is used to wire-bond at least one of the number of conductive layers to a gold wire.

77. A computer system comprising:

a processor;

a device coupled to the processor; and

a conductive structure coupled to the device, the conductive structure comprising:

a fine line having a layer of electroplated copper; and

a wide line having a number of conductive layers, at least one of the number of conductive layers is capable of eutectic bonding to a gold wire, and the wide line is coupled to the fine line.

78. A computer system comprising:

a processor;

a device coupled to the processor; and

a connective structure coupled to the device, the connective structure comprising:

a fine line having a single layer of electroplated copper having a depth greater than a critical depth; and

a wide line having a stack of conductive layers capable of eutectic bonding to a gold wire, and the wide line coupled to the fine line and the wide line having a depth greater than a critical depth.

79. A computer system comprising:

a processor;

a device coupled to the processor; and

a conductive structure coupled to the device, the conductive structure comprising:

a fine line having a depth greater than a critical depth and a single layer of electroplated copper; and

a wide line having a wide line depth equal to the depth, and a stack comprising a barrier layer, a copper layer, and an aluminum layer capable of eutectic bonding to a conductive material, and the wide line coupled to the fine line.

80. The computer system of claim 79, wherein the barrier layer comprises a refractory metal/refractory metal nitride.

Abstract of the Disclosure

An interconnect comprises a trench and a number of metal layers above the trench. The trench has a depth and a width. The depth is greater than a critical depth, and the number of metal layers is a function of the width. In an alternate embodiment, a metallization structure having a trench including a metal layer and a second trench including a plurality of metal layers coupled to the metal layer is disclosed. The metal layer is highly conductive, and at least one of the plurality of metal layers is a metal layer that is capable of being reliably wire-bonded to a gold wire. The trench is narrower than the second trench, and at least one of the plurality of metal layers is copper or a copper alloy.

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Printed Name Chris Hammond

Signature Chris Hammond

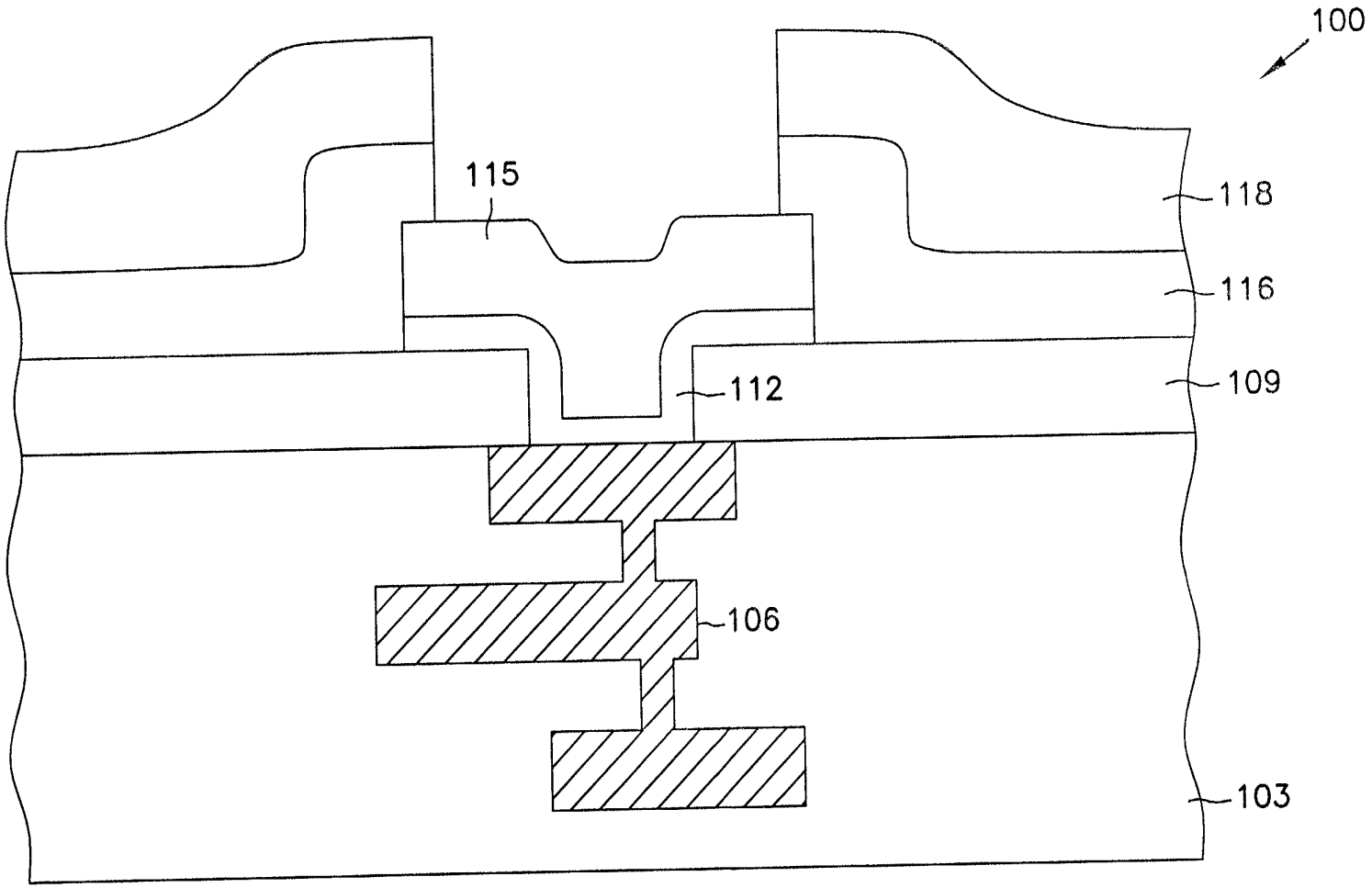

Figure 1 (PRIOR ART)

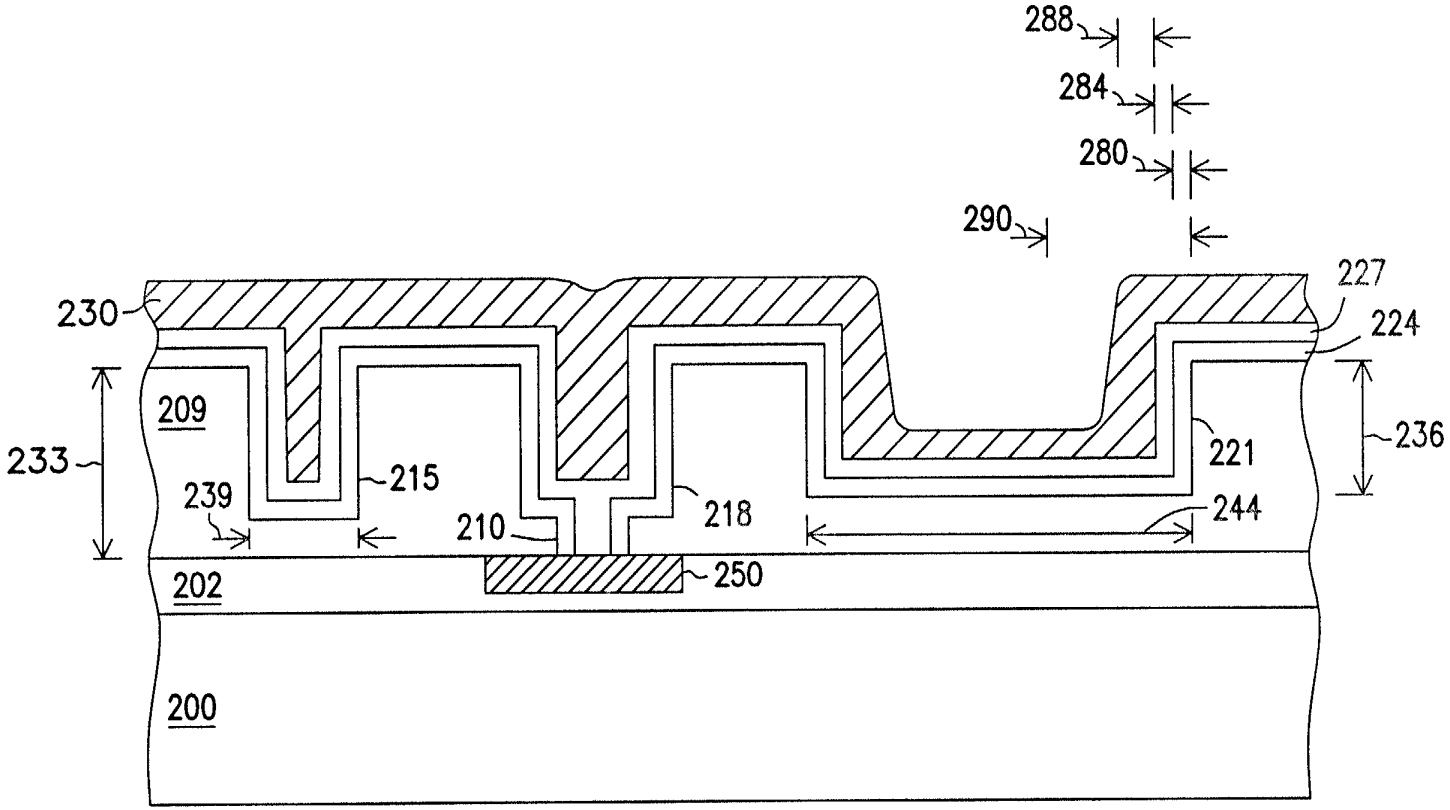

Figure 2

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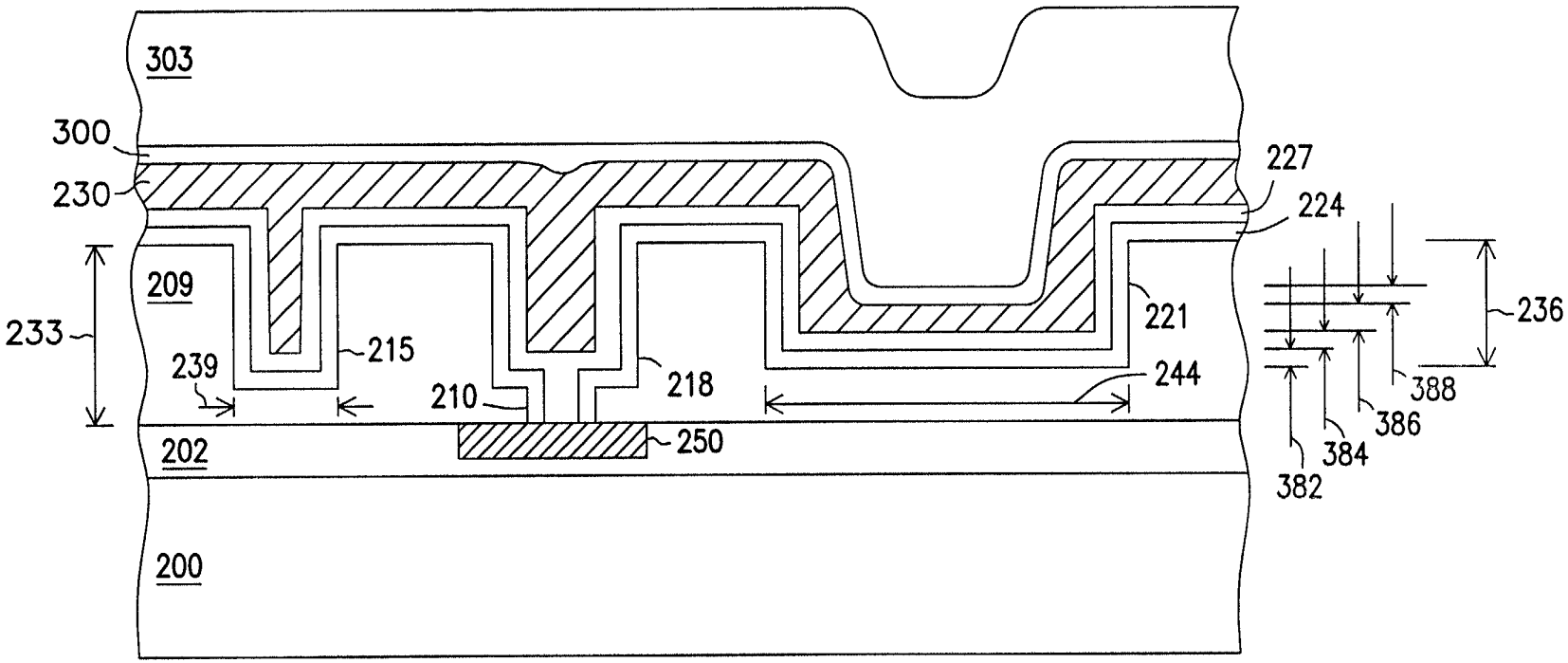

Figure 3

0038567 .0002

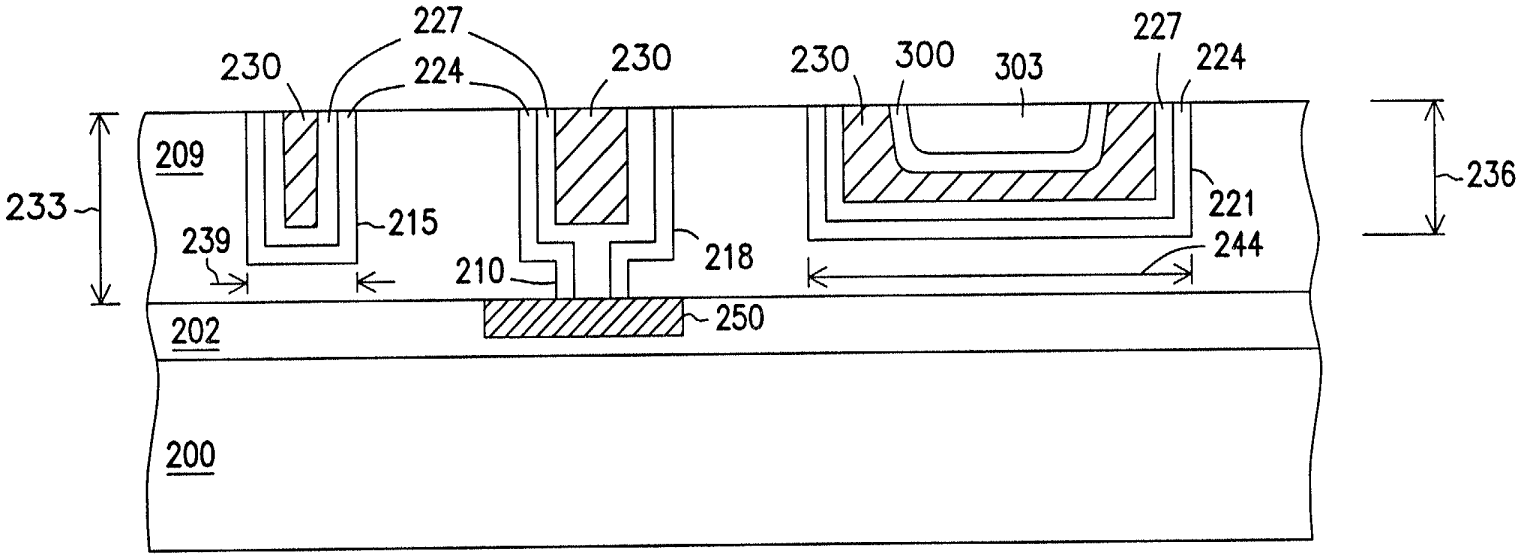
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Figure 4

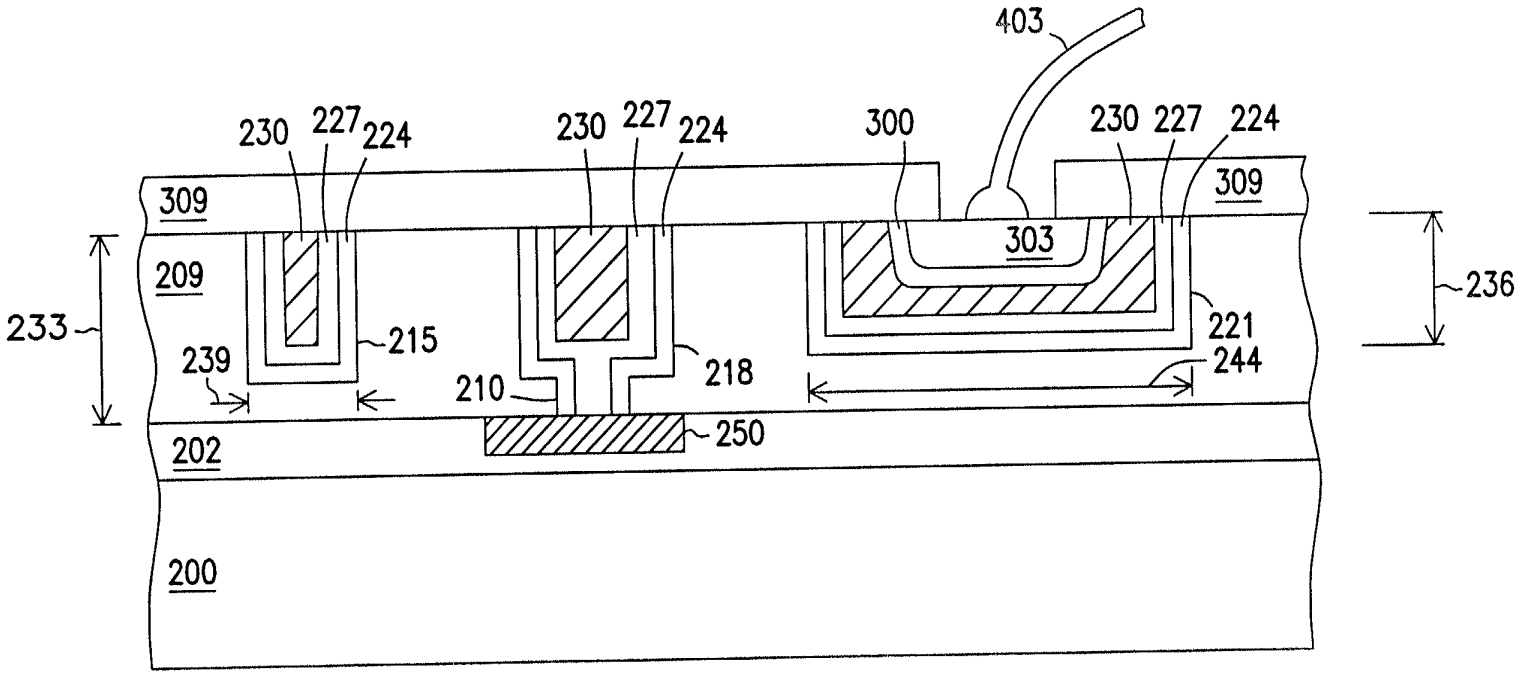

Figure 5

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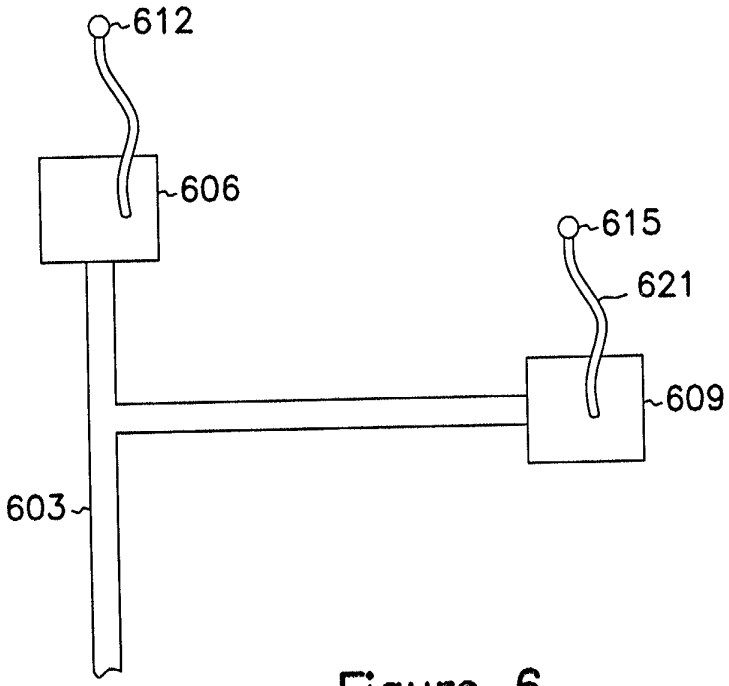
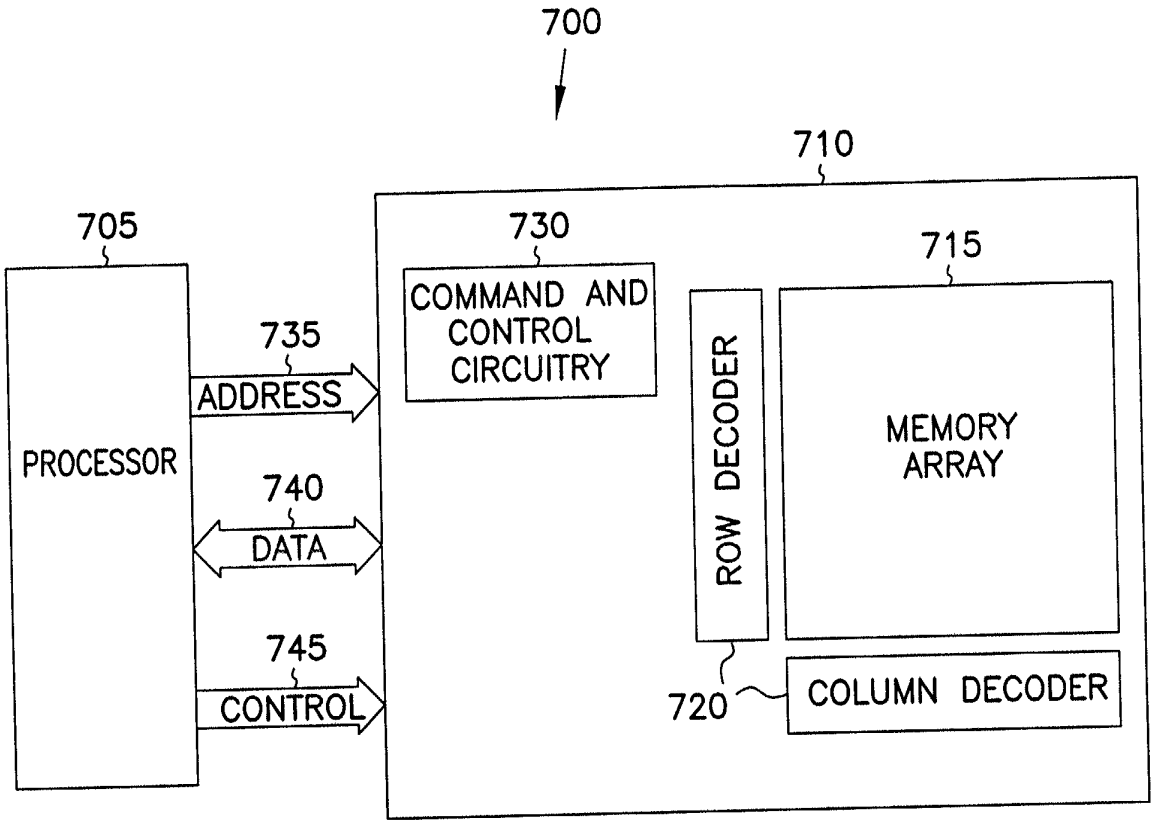


Figure 6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710
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730
715
COMMAND AND CONTROL CIRCUITRY
735
ADDRESS
PROCESSOR
740
DATA
745
CONTROL
ROW DECODER
MEMORY ARRAY
720
COLUMN DECODER

Figure 7

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

DECLARATION FOR PATENT APPLICATION

As a below named inventor I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled:

LOCAL MULTILAYERED METALLIZATION .

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56 (see page 3 attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, §119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

No such claim for priority is being made at this time.

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below:

No such claim for priority is being made at this time.

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application.

No such claim for priority is being made at this time.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of sole inventor : **Howard E. Rhodes**
Citizenship: **United States of America** Residence: **Boise, ID**
Post Office Address: 631 East Ridgefield Drive
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Signature: Howard E Rhodes Date: August 31, 1999
Howard E. Rhodes

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Post Office Address:

Signature: Date:

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: Date:

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: Date:

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§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is canceled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) it establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) it refutes, or is inconsistent with, a position the applicant takes in:

(i) opposing an argument of unpatentability relied on by the Office, or

(ii) asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application:

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.